

EAST - [400.wsp:1]

FileViewEditToolsWindowHelp

Drafts

BRS:

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L8: (51179) demultiplex\$3 or de adj multiplex\$3

L11: (182973) shifter or shift adj register or shift\$3 adj circuit

L12: (1527) 8 same 11

L13: (66) 11.ti. and 12

L14: (382) 11.ab. and 12

L15: (331) 14 not 13

L18: (45409) "377"/.ccls. or "708"/.ccls.

L19: (21) 15 and 18

L20: (5192) inver\$3 near1 order

L21: (10522) (revers\$3 or L20) near5 (bit or bits)

L22: (646) L21 with shift\$3

L23: (1) 15.and 22 not 19

708/200-656.ccls.

S1: (5186) inver\$3 near1 order

S2: (10511) (revers\$3 or S1) near5 (bit or bits)

S3: (646) S2 with shift\$3

S4: (214410) arithmetic or alu

S5: (45) S3 same S4

S6: (437455) feedback or feed back

S9: (15) S5 and S6

Query

Test

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DBs

US-PGPUB, USPAT, USOCR, EPO, JPO, DERWENT

Plurals

Default operator

ADJ

Highlight all hit terms initially

15 and 22 not 19

BRS form

IS&R form

Image

Text

HTML

	U	1	Document ID	Issue Date	Pages	Title	Current-OR	Current XRef	Re
1			US 5619722 A	19970408	24	Addressable communication port expander	710/2	710/300	

Hits

Details

HTML

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NUM

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UDC

L1: (5186) inver\$3 near1 order

L2: (10511) (revers\$3 or L1) near5 (bit or bits)

L3: (646) L2 with shift\$3

L4: (214410) arithmetic or alu

L5: (45) L3 same L4

L6: (437455) feedback or feed back

L7: (15) L5 and L6

L8: (26336) "708"/.ccls.

L9: (30) 5 not 7

L10: (71) 3 and 8

L11: (57) 10 not 5

L12: (11059) "712"/.ccls.

L13: (26) 12 and 3

L14: (6) 13 not (11 or 5)

L15: (22) 3.ti.

L16: (124) 3.ab.

L17: (96) 16 not (15 or 14 or 11 or 5)

Search

US-PGPUB, USPAT, USOCR, EPO, JPO, DERWENT

Plurals

Default operator: ADJ

Highlight all hit terms initially

BRS form

IS&R form

Image

Text

HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Re
1	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6163836 A	20001219	22	Processor with programmable addressing modes	712/37	712/209; 712/32;	
2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5987603 A	19991116	12	Apparatus and method for reversing bits using a shifter	712/300	708/209; 712/223	
3	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5926644 A	19990720	28	Instruction formats/instruction encoding	712/22	712/24; 717/149	
4	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 4931974 A	19900605	12	Sixteen-bit programmable pipelined arithmetic logic unit	708/521	708/508	
5	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 4075704 A	19780221	19	Floating point data processor for high speed operation	708/507	708/503; 708/505;	
6	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 5682340 A	19971028	13	Low power consumption circuit and method of operation for implementing shifts and bit reversals	708/209	377/54; 377/69;	
7	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 3768077 A	19731023	7	DATA PROCESSOR WITH REFLECT CAPABILITY FOR SHIFT OPERATIONS	708/200	708/625; 708/653;	

HitsDetailsHTML

NUM

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